WHITE PAPER

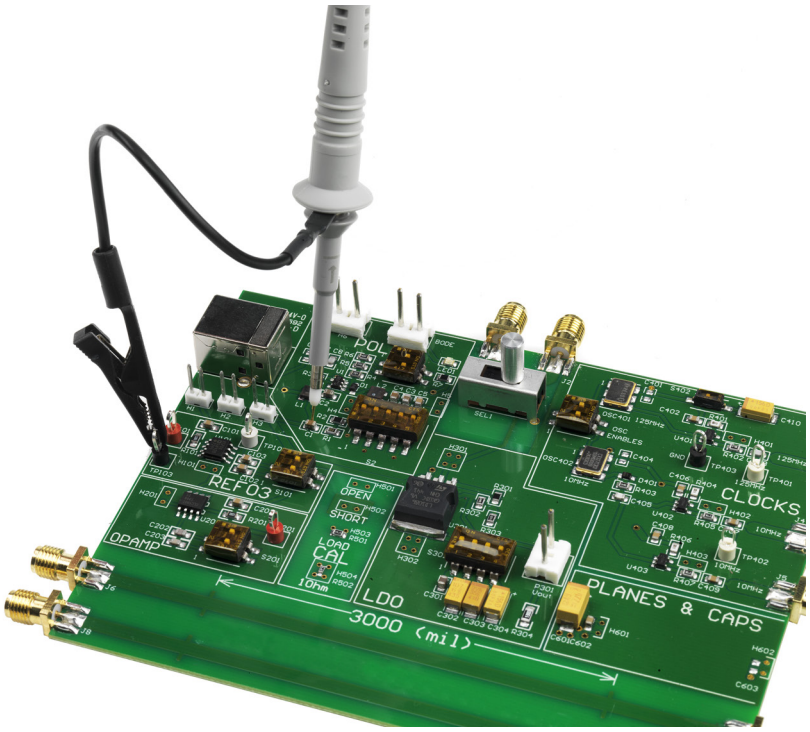
Journey of a Signal

What happens when you connect your oscilloscope probe to your device?

KEYSIGHT

The second you connect your oscilloscope probe to your device, your signal begins a journey that happens in the blink of an eye. It must pass through five different “blocks” to complete its journey from your device to the oscilloscope then back to the display.

This white paper explains everything your signal encounters along this journey to understand how a digital storage oscilloscope (DSO) works. Having this fundamental knowledge will help you make accurate measurements by correctly selecting the probes and oscilloscope that will work best for your test needs.



Block 1: Device Under Test (DUT) to the Front of the Oscilloscope

Your signal's journey begins with traveling from your device through a series of resistive and capacitive components inside the oscilloscope probe. Your probe's attenuation specification will determine what resistive components are inside. Figure 1 shows how most standard passive voltage probes have a 10:1 attenuation ratio.

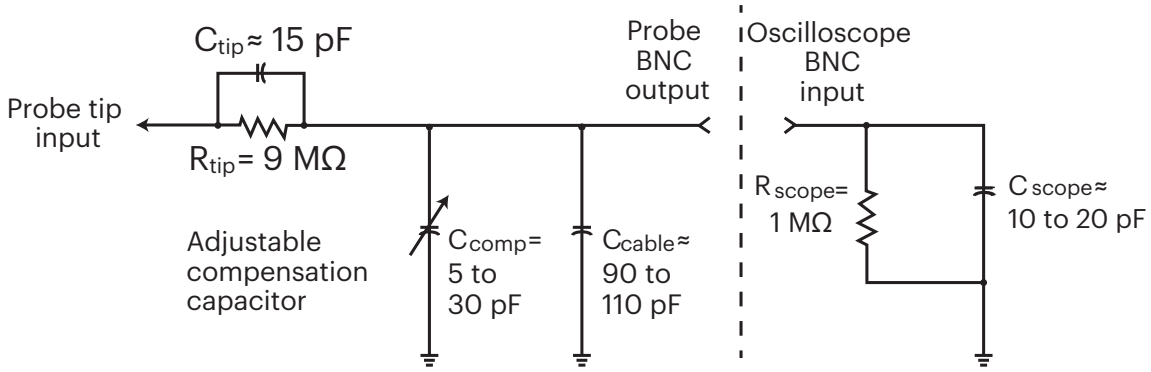


Figure 1. A 10:1 attenuation ratio probe design

This probe type has a 9 MΩ probe tip resistor in series with the oscilloscope's 1 MΩ input impedance, which makes the resistance at the probe tip 10 MΩ. When your signal travels through the probe and reaches the oscilloscope's input, it will be one-tenth of the voltage level that it was when it entered the probe at the tip of your device. This extends the dynamic range of the oscilloscope measurement system, enabling you to measure signals with a ten times higher amplitude than when using a 1:1 probe. The 10:1 passive probe also ensures a high input impedance at the probe tip, eliminating any loading on your device.

Block 2: Analog Input Signal Conditioning

The signal enters the oscilloscope to begin the first phase of processing: analog input signal conditioning. Figure 2 shows three stages to this conditioning process to scale the waveform correctly, so it is within the dynamic range of the analog-to-digital converter (ADC) and the amplifier.

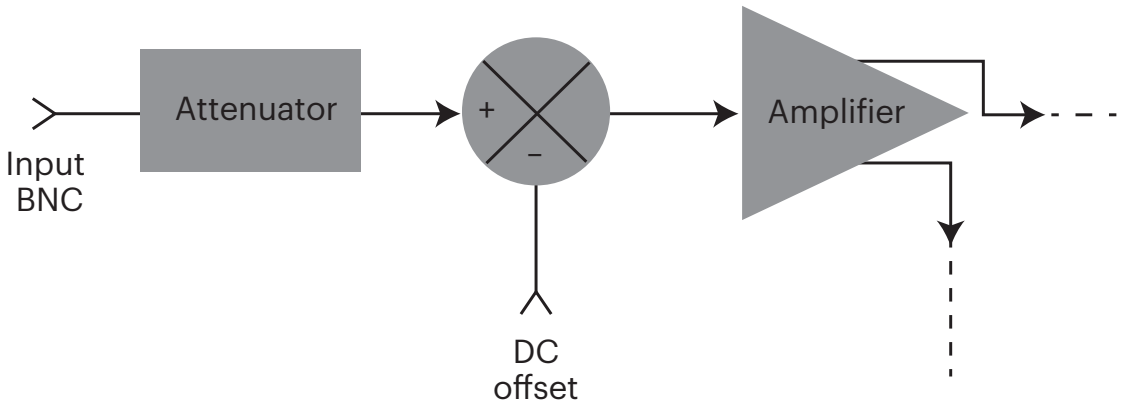


Figure 2. Three stages of the analog signal conditioning block

The processing in these stages is dependent on the V / div and offset settings and whether you are measuring a low- or high-level signal. The attenuator block is a network of resistor dividers that scales the signal. When you have a high-level input signal, the signal is attenuated (or reduced). If you input a low-level signal, the signal will pass through to the next step without any attenuation.

You may require inputting a signal that has a DC offset. Still, you want to be able to display that signal in the center of the screen at 0 V. The oscilloscope has an internal DC offset of the opposite polarity to the signal to shift the scale to make this happen. This functionality displays the signal in the center of the screen.

The signal then travels into the variable gain amplifier. This type of amplifier will either increase or decrease the gain of your signal depending on the V / div setting. This setting depends on whether you are looking at a low- or high-level signal. You are probably using a low V / div setting that tells the amplifier the gain needs to increase to use the full range of the ADC when working with a low-level signal. If you are working with a high-level signal, the attenuator would have reduced the signal in the first stage of the process. The amplifier may then further attenuate the signal in this stage by decreasing the gain to scale the signal within the dynamic range of the ADC.

Block 3: Analog-to-Digital Conversion and Trigger

The conditioned signal is within the ADC's dynamic range and can now enter the center of the oscilloscope so that the analog-to-digital conversion can begin, as shown in figure 3. The ADC block is the core component of DSOs.

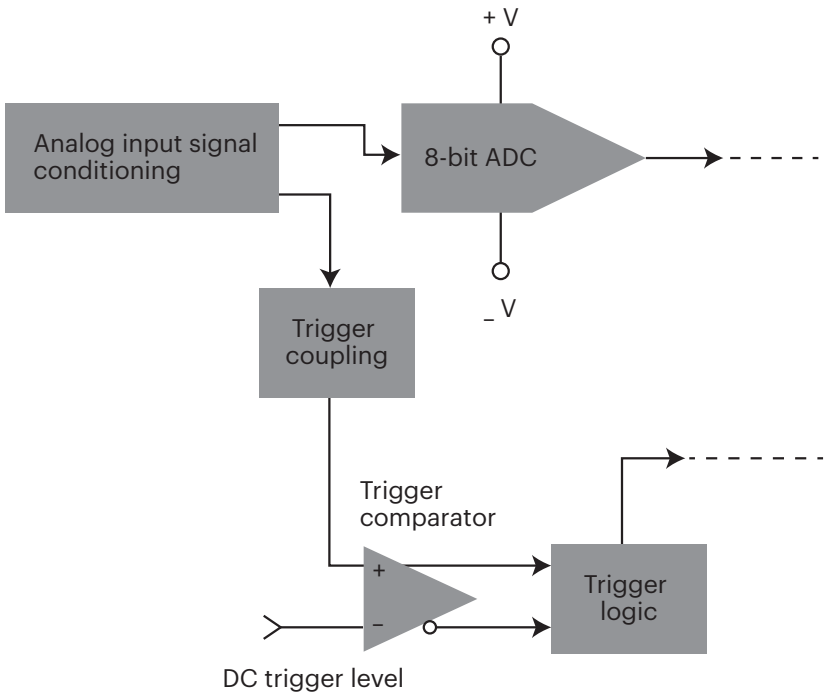


Figure 3. The analog-to-digital conversion and triggering system

Figure 3 is where the analog input signal undergoes conversion into a series of digital words. Most of today's DSOs use 8-bit ADCs that provide 256 unique digital output levels/codes, which are stored in the oscilloscope's acquisition memory. The oscilloscope will try to use the full dynamic range of the ADC to obtain the highest resolution to ensure accurate measurements. While the ADC converts the signal, the oscilloscope also processes the trigger conditions needed to establish a unique point in time on the input signal to achieve a synchronized acquisition.

Depending on the oscilloscope's trigger acquisition settings, the trigger comparator block will output a non-inverted waveform with a duty cycle that is dependent on what you set the trigger level to. Then, depending on the trigger type (rising edge, falling edge, etc.), the trigger logic block will either invert the waveform or allow the non-inverted waveform to pass through to the next step to use the signal as the unique synchronization point in time.

Block 4: Time Base and Acquisition Memory

Figure 4 shows that the time base block controls when the ADC sampling starts and stops relative to the trigger event determined in the previous step. The time base block also controls the ADC's sample rate based on the oscilloscope's available acquisition memory depth and the time base setting.

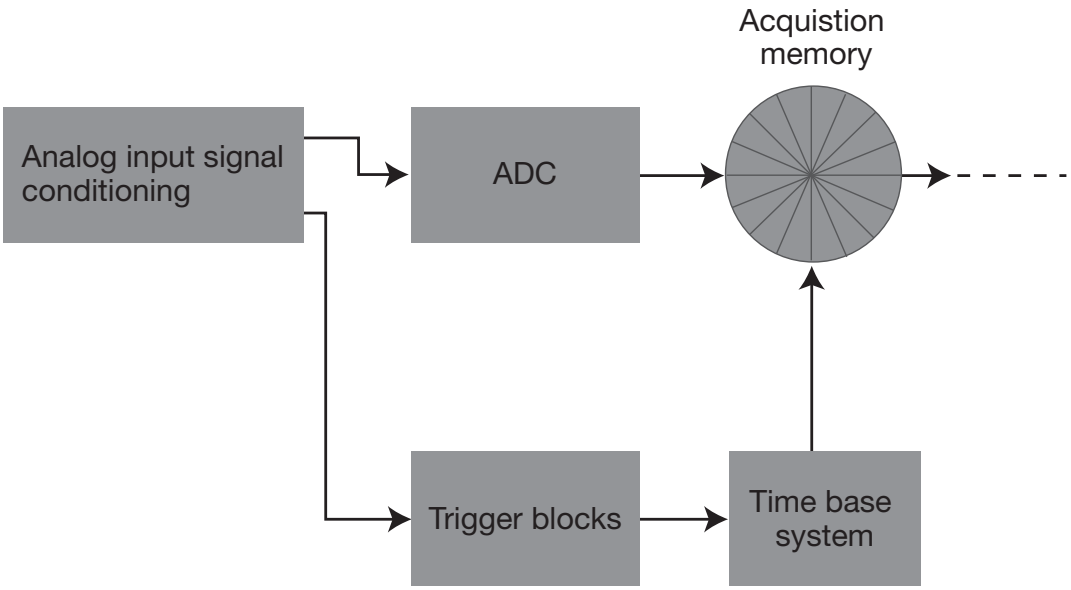


Figure 4. The time base system and acquisition memory process

After pressing the run key, the time base block enables continuous storing of the digitized data into the oscilloscope's "circular" acquisition memory at the appropriate sample rate.

While the time base block increments address the circular acquisition memory buffer after each sample, they also count the number of samples taken up to a certain number. This number depends on the oscilloscope's memory depth along with the trigger position.

The time base block enables triggering and begins to look for the first qualifying point of the output trigger comparator once the time base block collects the minimum number of required signal samples.

The time base block then begins collecting the required number of samples once it detects the trigger event. Once it stores all the samples, the time base block disables the sampling, and the process pushes to the next step.

Block 5: Display Digital Signal Processing (DSP)

Your signal has now reached the final stage in its journey. The data in the acquisition memory withdraws in a last-in-first-out sequence once all of the samples have been acquired. The signal is then reconstructed from the samples, and the data is pushed to the oscilloscope's pixel display memory, where you can now view the results on the screen, as shown in figure 5.

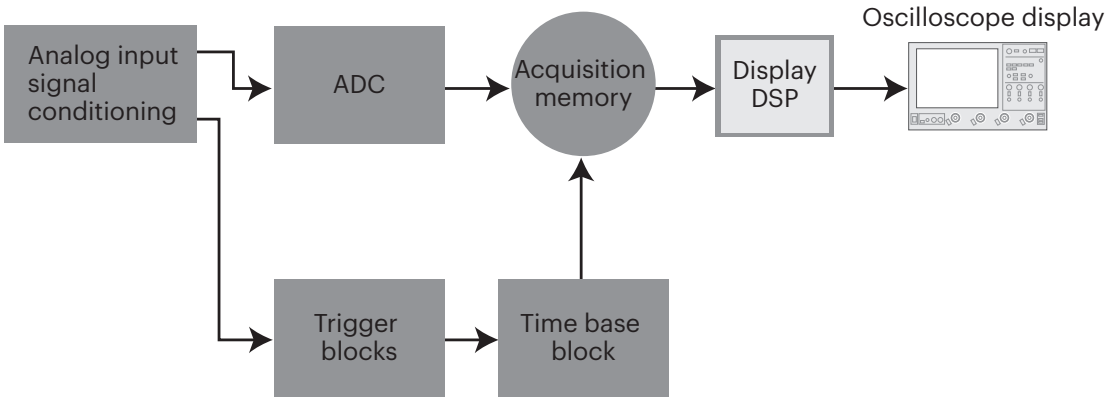


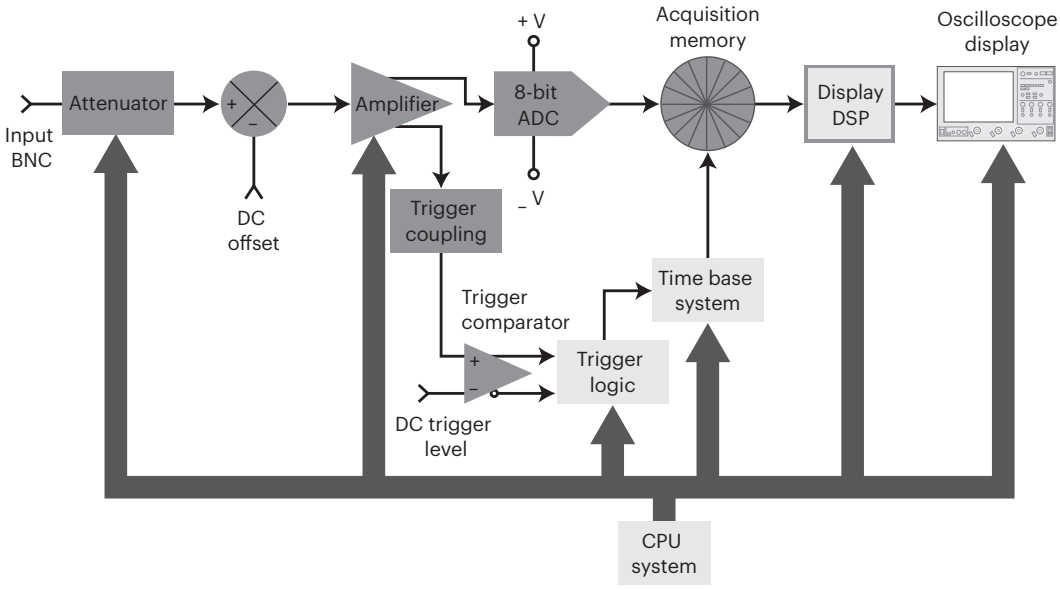
Figure 5. The digital signal processing block display process

Once all the data withdraws from the acquisition memory, the DSP block signals the time base block that it can begin another acquisition. This is a technique that is unique to Keysight's custom ASIC technology.

Traditionally, other digital storage oscilloscopes would not include this DSP block. Instead, they would use the oscilloscope's central process unit (CPU) system, as shown in Figure 6. That method greatly decreases the oscilloscope's efficiency and slows down the waveform update rate, which causes you to lose accuracy in your measurements and miss important anomalies.

Using the DSP block enables Keysight oscilloscopes to operate at a high efficiency and display a truer waveform to what is actually coming from your device.

DSO Block Diagram



You can see the signal goes through quite a long journey before it appears on the oscilloscope's screen; however, this all happens in the blink of an eye.

To learn more about how an oscilloscope works, check out the 6 Essential Tips for Getting the Most Out of Your Oscilloscope eBook. Also, don't forget to download a free copy of The Journey of a Signal: Inside your Oscilloscope poster!